THIN-FILM INTRACORTICAL RECORDING MICROELECTRODES

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Center for Wireless Integrated MicroSystems
Department of Electrical Engineering and Computer Science
The University of Michigan
Ann Arbor, Michigan
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Summary

During the past quarter, we have continued to improve our packaging techniques for chronic recording probes and have begun, working with the Center for Neural Communication Technology, to explore the tissue reaction to chronically implanted probes using a new round of histological studies. We have also begun to design narrow-shank recording probes using both single-crystal silicon and polysilicon shank structures. The anticipated probes will have multiple shanks, each about 3µm wide, with recording sites that overhang the shank to allow full-field recording in-vivo. The chronic behavior of the new sites will be studied in the potential field of single cells.

Fabrication has been completed through final release on a samples of the most recent probe designs. The wafer yield was excellent, with very few broken shanks and almost no evidence of circuit undercutting. Probes appear to be functioning as designed, with several probes bonded and in-vitro and in-vivo testing underway. Release on standard probe designs is now straightforward; however, care must be taken in probe placement on the wafer and in the release etch when shank spacings less than 150µm are used. A dry silicon etch is one approach that has been found effective in fabricating the smaller structures. Gold shields have been fabricated over the circuit areas of some of the new active probes. The circuitry is functional and these probes are being applied to long-term testing in-vivo and (at higher temperatures) accelerated testing in-vitro.

In releasing some of the active probes, problems with metal spikes remaining at the patterned metal edges after lift-off have been seen. Extensive photoresist studies of the line edges during lift-off have been carried out and have suppressed these problems adequately to achieve acceptable probe yields. A new photoresist specifically designed for use in lift-off processes has also been obtained and will be explored as a more complete solution to the problem.

Wafer level testing of the newly-designed active probes (PIA-2) has produced very promising results. The counter used to control the time-division multiplexer is fully operational along with associated logic gates and CMOS switches. The capacitively-coupled PIA-2 on-chip amplifiers have also been tested at the wafer level. The in-band gain is 39.5dB with an upper cut-off frequency of 40kHz. The low frequency cut-off is below 10Hz; the amplifier can reject greater than ±400mV DC at its input. Design of a platform-mounted integrated circuit that will perform neural spike detection based on a user-input threshold is also nearing completion. It is being designed in an AMI 0.5µm CMOS process and will be fabricated as part of a MOSIS run starting late next month. Finally, the sigma-delta modulator to be used in the first recording probe telemetry interface has been analyzed. The circuit dissipates 230µW and produces 8b resolution for x32 oversampling. We are developing a 1mW Colpitts transmitter that is expected to achieve a bit rate of 1.6Mb/s for 8-channel neural recording.

Thin-Film Intracortical Recording Microelectrodes

1. Introduction

The goal of this program is the realization of batch-fabricated recording electrode arrays capable of accurately sampling single-unit neural activity throughout of volume of cortical tissue on a chronic basis. Such arrays will constitute an important advance in instrumentation for the study of information processing in neural structures and should be valuable for a number of next-generation closed-loop neural prostheses, where stimuli must be conditioned on the response of the physiological system.

The approach taken in this research involves the use of solid-state process technology to realize probes in which a precisely-etched silicon substrate supports an array of thin-film conductors insulated above and below by deposited dielectrics. Openings in the dielectrics, produced using photolithography, form recording sites which permit recording from single neurons on a highly-selective basis. The fabrication processes for both passive and active (containing signal-processing circuitry) probe structures have been reported in the past along with scaling limits and the results of numerous acute experiments using passive probes in animals. In moving to chronic implant applications, the major problems are associated with the preserving the viability of the sites in-vivo (preventing tissue encapsulation of the sites) and with the probe output leads, both in terms of their number and their insulation. The probe must float in the tissue with minimal tethering forces, limiting the number of leads to a few at most. The encapsulation of these leads must offer adequate protection for the megohm impedance levels of the sites while maintaining mechanical lead flexibility.

Our solution to the lead problem has involved two steps. The first has been to embed circuitry in the probe substrate to amplify and buffer the signals and to multiplex them onto a common output line. Using this approach, signal levels are increased by factors of over 100, impedance levels are reduced by three to four orders of magnitude, and the probe requires only a few leads for operation, independent of the number of recording sites. A high-yield merged process permitting the integration of CMOS circuitry on the probe has been developed, and this circuitry has been designed and characterized. The second step has involved the development of silicon-based ribbon cables, realized using the same probe technology, to conduct the neural signals to the outside world. These cables have shown significant advantages over discrete leads, both in terms of the ease with which chronic implants can be assembled and in terms of the ability of the cables to survive long-term biased soaks in saline. The cables can be built directly into the probes so that they come off of the wafer as a single unit, requiring no joining or bonding operations between them. The cables are also significantly more flexible than previously-used discrete wire interconnects.

This contract calls for the development of active probes for neural recording. A 64-site 8-channel probe with site selection and signal buffering but no multiplexing has been developed (PIA-2B) along with a high-end multiplexed probe that includes gain

(PIA-2). These probes are now being refined and applied to in-vivo applications. Investigations are on-going to better understand site encapsulation, which limits the lifetime of chronic recording structures, and telemetry is being developed to allow the probes to be operated over a wireless link, eliminating the percutaneous connector.

During the past quarter, we have continued work on reducing the size of the recording probe shanks and have completed final release on a new set of active probes (PIA-2B and PIA-2/-3). We are nearly complete with the design of a platform-mounted spike recognition circuit for the probes as well as a wireless interface for them. Work in these areas is discussed in the sections below.

2. Chronic Studies with Passive Recording Probes

One of the important parts of this research is learning how to optimize the chronic recording capabilities of these probes, and that depends critically on packaging. During the past quarter we have encountered problems with the packaging of the chronic 32-channel electrode placed in guinea pig inferior colliculus (Fig. 1). These problems led to breakage during implantation and movement of the electrode once implanted. We are currently in the process of redesigning the way it is packaged and expect the redesigned probe to function well on a chronic basis in terms of its packaging.

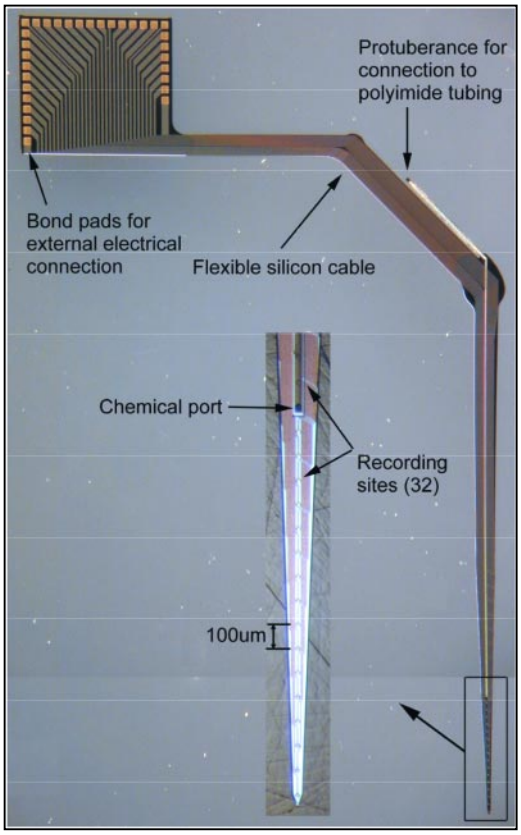

Fig. 1: A box-beam probe design that can also be used for chemical delivery.

In conjunction with the Center for Neural Communication Technology (CNCT), we began a study last quarter to examine the composition of the envelope which often surrounds chronically implanted electrodes through the use of immunohistochemistry (Table 1). This study is still ongoing; histological results should be available next quarter.

Antibody	**Used to Identify**
GFAP	Astrocytes/Glia
Vimentin	Connective Tissue
OX-42	Macrophages, Monocytes, Granulocytes
Fibronection	Extracellular Matrix-Epithelial
Laminin	Extracellular Matrix-Neuronal
NeuN (MAB 377)	Neurons
MAB 328	Oligodendrocytes

Table 1: Antibodies specific to specific physiological features in probe sheath analysis.

We have also started to chronically implant 32-channel brain-in-the-box electrodes into guinea pig auditory cortex. This electrode design has two parallel planes of four shanks each, whose sites face each other allowing for imaging a block of neural tissue (Fig. 2).

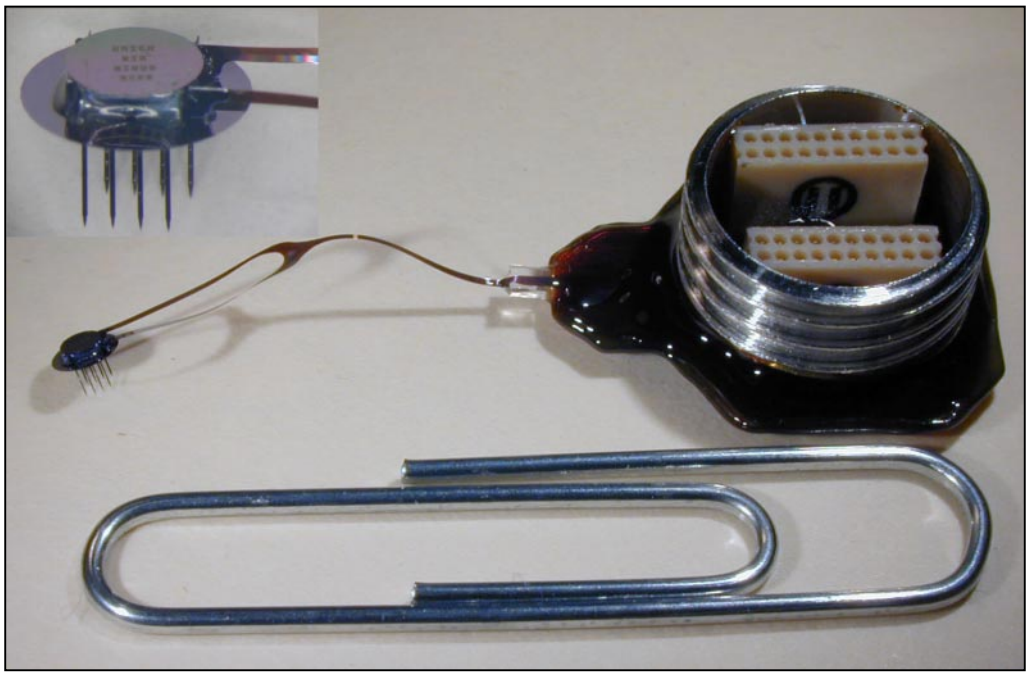

Fig. 2: Fully-connected 32-channel brain-in-the-box probe. Each of the eight shanks has four sites.

Training:

One of the goals of these studies and especially through the CNCT is to provide training to outside investigators who want to use the Michigan probes. Professor David Martin of the Material Science and Engineering Department here at the University of Michigan has started a contract affiliation with Patrick Fresco's group at the University of Utah to examine the biological response of coated probes in-vitro and in-vivo. Dr. Tresco and colleague, Roy Biran, recently came to receive training in chronic implantation of the Michigan probes. This collaboration with Material Science and Engineering and CNCT should greatly enhance our understanding of why chronic electrodes degrade in performance over time. More importantly, countermeasures may be developed from these collaborations that will expand the life of our implants.

5. *Scaled Recording Probe Development*

Recording studies call for an increasing number of sites, and to minimize the tissue trauma associated with array insertion and residence, it is important that the shanks be as small as possible. In the past, we have demonstrated that shanks can be made much narrower than our standard dimensions (50-80μm), and we are now developing techniques for reducing shank widths considerably. Such "nanoprobes" should minimize tissue damage, allowing recordings from multiple sites within the field of a single cell as well as the transparent spacing of sites throughout a block of relatively-undisturbed neural tissue.

Two structures for cellular probes that minimize tissue displacement and yet allow extracellular recording/stimulation (along with possible intracellular recording, stimulation, and chemical delivery) are being explored. The first structure, a U-shaped probe (Fig. 3) is fabricated by etching two trenches along the two sides of the shank using RIE. This occurs after a normal probe fabrication but before contacts and metal. The trench is then refilled with polysilicon to allow subsequent lithography. Contacts are opened and the site metal is deposited to overhang the narrow shank. The overhang and narrow shank should allow recording from a nearly spherical space around the probe with little shadowing from the substrate.

A second T-shaped probe structure (Fig. 4) uses a single trench that is oxidized to form a diffusion barrier and then partially refilled with polysilicon at the start of the process. The polysilicon is boron diffused and then oxidized prior to completion of the trench refill with polysilicon. Contacts and metal are then deposited to complete the process. The final structure is similar to the U-shaped design but the probe body is polysilicon with an oxide core. This may make stress compensation more difficult but it more closely resembles a box-beam probe and should be strong. If the polysilicon is removed sacrificially from the core of the probe, a natural flow channel is formed for drug delivery as well. Both structures minimize the volume displacement of the microprobe while preserving reasonable site areas. Recording studies have indicated that

preferred site sizes for recording should be around 400~600μm^2 (rather than the more typical 100μm^2 we have used in the past). Thus, with a shank size of 3μm and a recording site diameter of 25μm, the site overhang would be about 10μm and it will record as if double-sided.

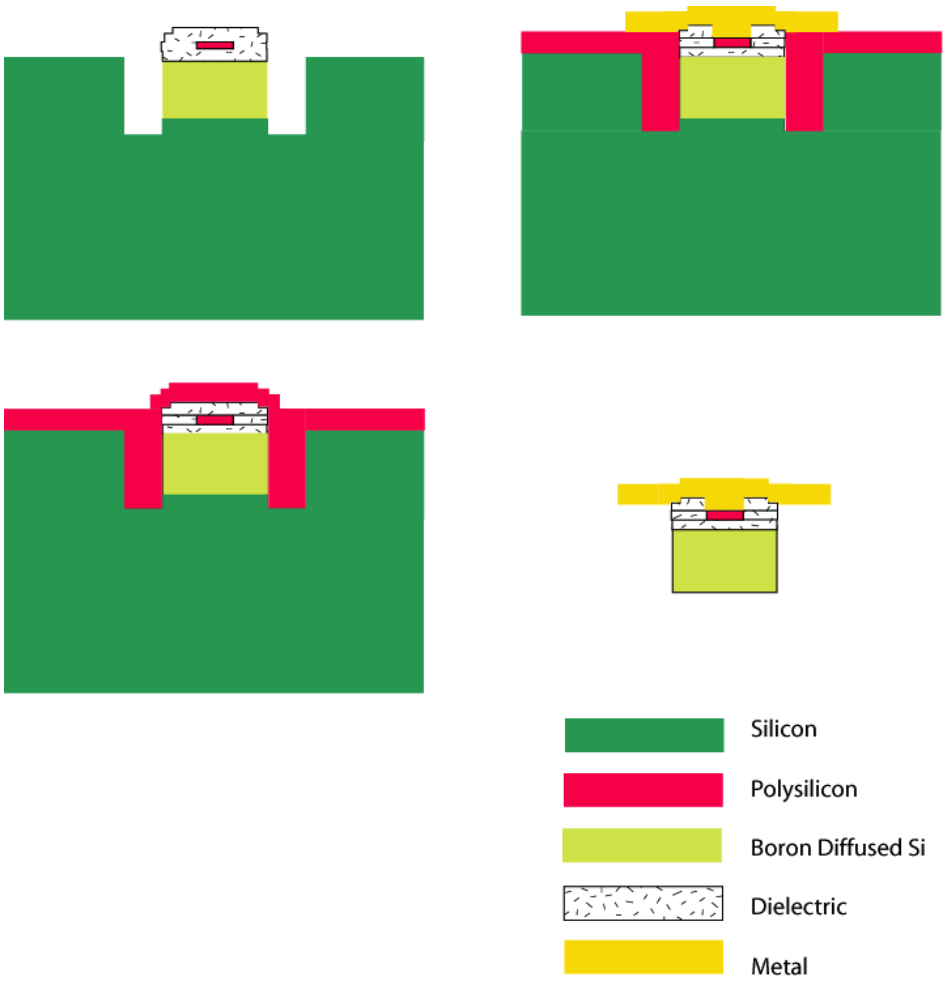

Fig. 3: Fabrication sequence for a U-shaped probe shank

We are in the process of designing a mask set to explore these two approaches to smaller shanks experimentally. The probes will consist of multishank designs consistent with recording from within the field of a single cell. We also hope to compare the recording characteristics with our standard shank designs by fabricating some of these structures on the same mask set. Another issue concerns the strength and the stiffness of the narrower probes as their shank widths decrease. It is required not only that the probes be strong enough to avoid breaking, but that they should also be stiff enough to avoid excessive bending. The shanks should be at least 1~2mm long, 3~4μm wide, and 5~6μm thick. We will check to see if such silicon substrates are strong enough for our applications. For U-the shaped probe, it could be easier to estimate the strength and stress of probe than for T-shaped because the T-shaped probe is fabricated using a polysilicon shank, which is less well characterized mechanically than single-crystal silicon.

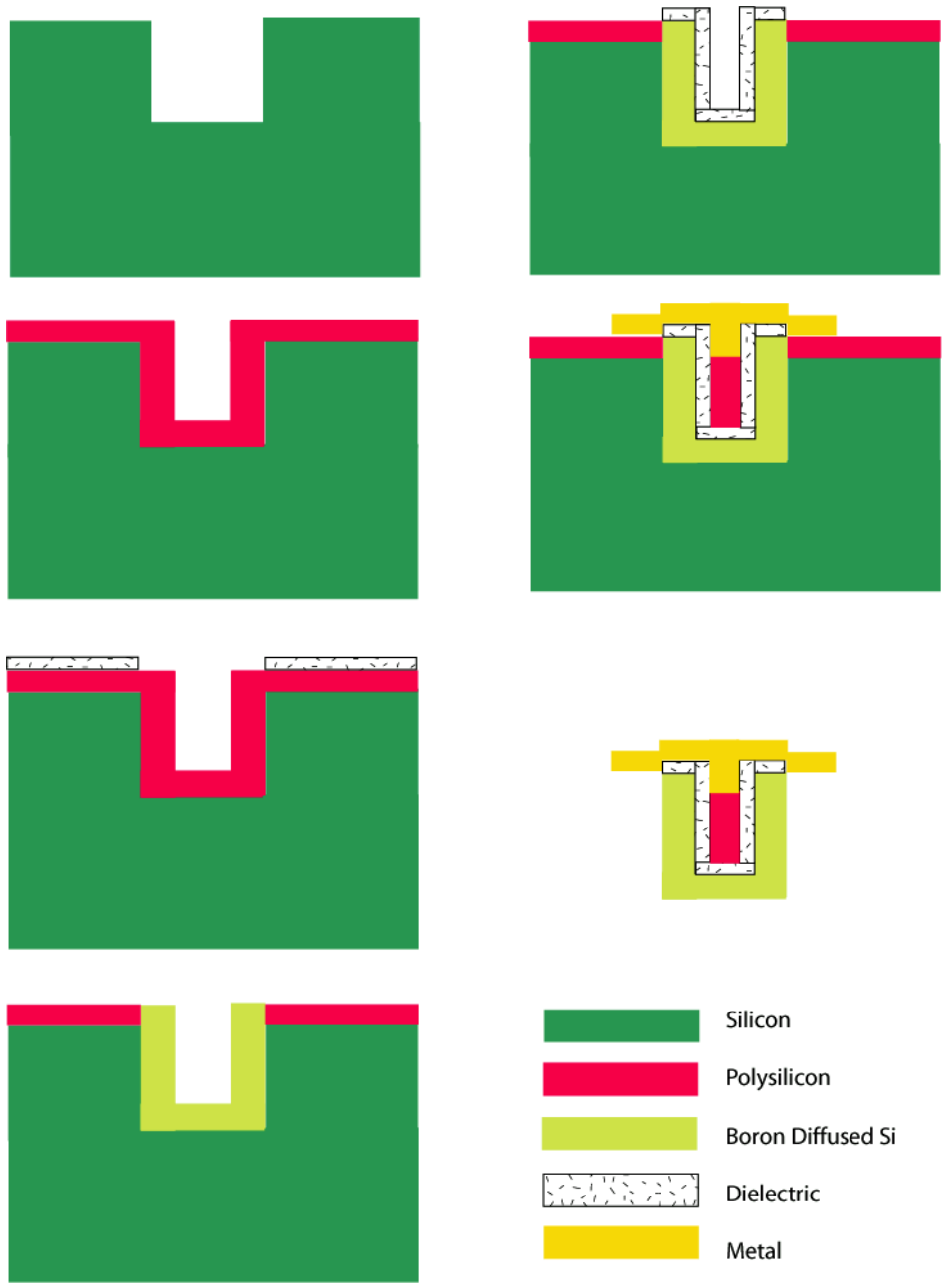

Fig. 4: Fabrication sequence for T-shaped probe shank

In order to quantitatively analyze the strength of these probes, at least two parameters have to be determined: the maximum load (force) required to buckle the probe shank (which determines the stiffness of the probe shank), and the maximum fracture stress of thin silicon (boron diffused) substrates (which determines the strength of the shank after it buckles). These two parameters can be calculated from two equations:

$$P = \frac{2EI\pi^2}{L^2}$$

$$\sigma_{\max} = \frac{6Ehu}{L^2}$$

The first equation is for the buckling load and is obtained using mechanical theory of columns, where E is the Young's modulus (1.7×10^{12} dynes/cm^2 for silicon), I is the moment of inertia of the area, L is the length of the column, and P is the buckling load. Because the moment of inertia of the area is different for different cross-sections, the approximation of the cross-section is important to get the buckling load. For both probe designs, the cross-section can be taken to be rectangular.

The second equation defines the fracture stress of the shank and hence the probe strength, where h is the shank thickness and u is the maximum amount of lateral deflection of the buckled shank. After calculating the parameters from each design, we can roughly optimize the size of the probe and the thickness of each deposited material. These equations will be used to simulate the two designs and to compare their measured strength when fabrication has been completed. We hope to have samples of each probe by summer.

4. Development of a 64-Site Eight-Channel Non-Multiplexed Recording Probe (PIA-2B)

Fabrication has been completed on a single wafer of the most recent probe designs. The wafer yield was excellent, with very few broken shanks and almost no evidence of circuit undercutting. Probes appear to be functioning as designed, with several probes bonded and in-vitro and in-vivo testing underway. Testing of all of the designs on the current fabrication run, which have been described in previous quarterly reports, is expected to continue for at least the next quarter.

In the last quarter we reported that fabrication had been completed through circuit metal. Measured process parameters agreed well with expected values, and the performance of all circuit blocks had been verified. Efforts over the past three months have been aimed at completing final processing on these wafers and etching out active probes for in-vivo experimentation. Several challenges have been encountered which have led to the redesign of several masks and changes to the circuit metal and electroplating processes. These challenges and their proposed solutions will be addressed in the following subsections.

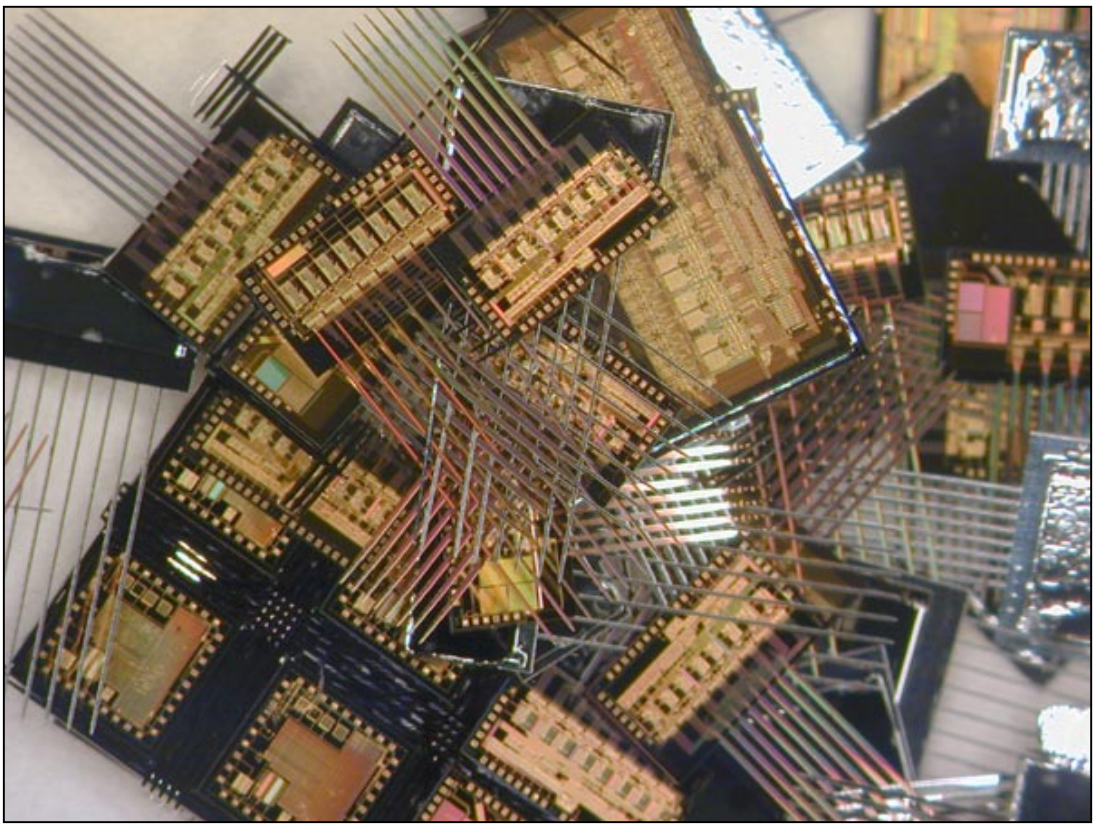

Fig. 5: Completed probes after release from wafer.

4.1 Dielectric Mask and Final Release in EDP

The current fabrication run is composed of two separate mask sets due to the large number of designs present. One mask set contains standard probe shapes and designs, while the second contains mostly probes that are unusual in some respect and may require special processing for release from the wafer. This includes active probes with integrated ribbon cables, probes with small inter-shank spacings, exceptionally large probes, as well as chronic probes with wings for beam-lead transfers. The standard probe shapes, as shown in Fig. 5 above, etched out as expected with very high yield. The second mask set has been more of a challenge, and test etches with dummy devices have been carried out in advance of final device release in order to test the dielectric mask.

The active probe process relies on backside EDP etching to undercut (and clear) the shanks, chronic probe wings, and ribbon cables. Undercutting of these areas occurs when the back-side etch meets the front-side etch, exposing a corner which is attacked rapidly by EDP. Undercutting of the circuit areas by the same process competes with the necessary etch-back to the boron etch stops. The process window for successful release (i.e., cleared shanks without undercut circuits) is determined by the difference in spacing

between the shanks and probe bodies, which determines the ultimate depth of the front-side etch before stopping on the (111) planes. Further control over the front-side etch is achieved with corner compensation and dielectric etches, which can also be used to adjust device spacing as necessary.

Figure 6 below shows a large chronic probe which was designed with integrated ribbon cables separating the shanks and wings from the circuit area, allowing it to fold over onto a 3D platform. It can be seen that utilizing the standard active probe release process, the etch-stop was reached in the wings, shanks, and ribbon cable while most of the circuit area remained unattacked. This is an encouraging result, especially in light of the fact that the process window was purposely exceeded to test the limits of the dielectric mask. However, it can be seen that the corners and back edge of the circuit area were attacked. The dielectric mask was changed to add additional corner compensation and bridges in order to solve this problem. Similar problems were found with probes designed with integrated ribbon cables for chronic implantation, and adjustments were made to the dielectric mask.

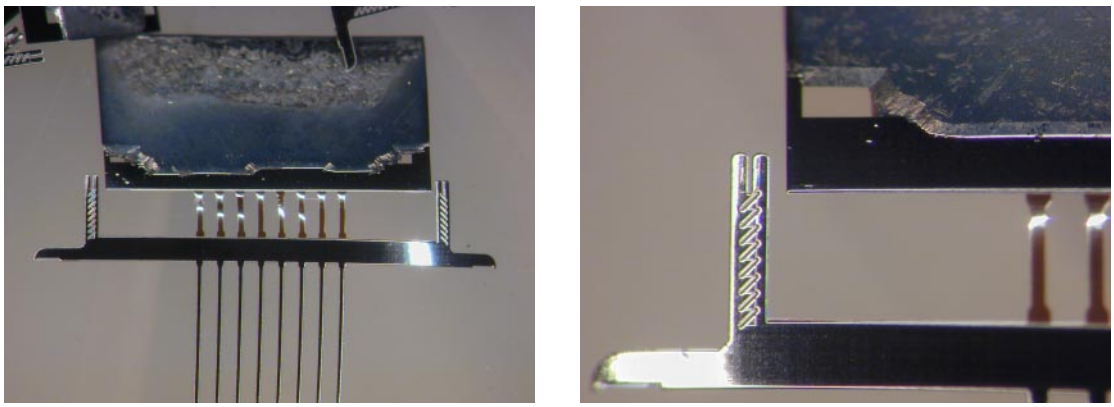

Fig. 6: Released probe with integrated ribbon cables for folding over of circuit. Bucking in shanks is due to the lack of stress compensation in dielectric stack; this is a test device.

The test etches of these unique structures highlight the strengths and limitations of the current active probe release process. When probe designs are standard (i.e. rectangular circuit area, widely spaced shanks) etch out is highly predictable and yield is excellent. As these limits are pushed, however, it becomes more difficult to predict etch-out exactly, and an iterative process of test etches and dielectric mask redesigns becomes necessary. Further, as the number of designs increases, it becomes more difficult to place the probes on the wafer in ways that allow a high device density (and thus yield) while maintaining control of the etch. This is a result of the fact that large areas that must be cleared on one design (i.e., wings, shanks, cables) require a large front-side pit. This may cause problems, however, with adjacent probes that will be undercut due to the presence of the large adjacent pit. The choice is either to increase the dielectric padding around each probe (and thus sacrifice yield- not desirable as the size and number of different

probes increases) or else to carefully consider the placement of each probe relative to others.

Another limitation of the back-side undercutting of structures is that it is difficult to release active probes with shank spacings narrower than 150µm or so due to the process window needed with circuit area release. Because there is now a deep RIE etcher in-house, the use of trenches to undercut shanks and other structures from the front-side is a simple and readily available remedy for to the reliance on the backside etch, and results in an increased process window. Etching a 70µm trench provides roughly 50µm of lateral undercut. If this is done on both sides of a shank or ribbon cable we can clear structures up to 100µm wide from the front-side – wide enough for most shanks and ribbon cables. This technique was used on a test wafer for releasing probes with 40-70µm shank spacing, and excellent results were obtained. To take full advantage of this technique, one would want to increase the inter-probe wafer spacing and rely entirely on front-side undercutting through the appropriate choice of DRIE mask design and etch depth.

4.2 Electroplated Gold Circuit Shield

In order to provide circuit encapsulation for chronic implantation of active probes, a 3µm-thick gold shield was electroplated over the circuit area of the active probes.

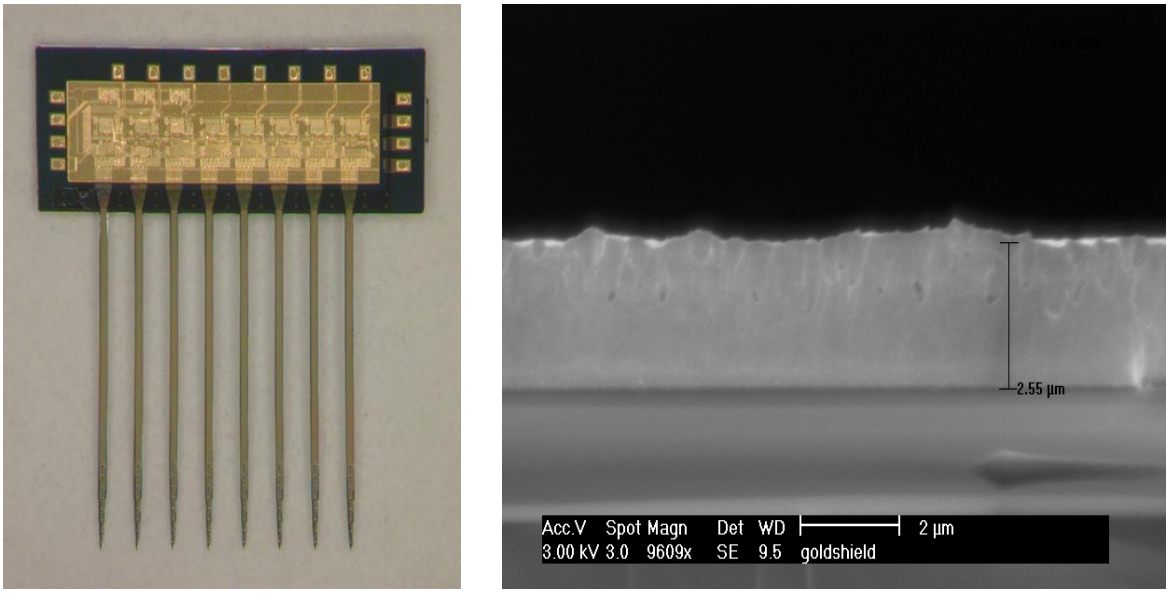

Fig. 7: Probe with electroplated gold shield over circuit area, left. Cross section of gold film, right.

Two methods of electroplating the shield were initially tested. In the first method, a seed layer of chrome/gold/chrome was sputtered onto the wafer. A single dark field

mask was then used to pattern thick photoresist in the circuit areas and the gold bond pads. Electroplating for roughly thirty minutes at a current density of $0.5mA/cm^2$ was then carried out to produce bond pads and a circuit shield. Finally, the seed layer was etched back in the non-electroplated areas. During etch-back, the dark field plating mask must be reversed and applied to protect the plated gold. Although the plated gold layer is much thicker than the seed layer, the presence of gold spikes can provide a means for the gold etchant to attack the underlying layers if this is not carried out.

The second electroplating method utilized a chrome/gold seed layer that was then patterned using a clear field mask. The gold was etched back everywhere but in the circuit and bond pad areas. The photoresist was then stripped and electroplating was carried out. Because chrome oxidizes rapidly, the exposed chrome is passivated and gold is not plated in these areas. This method has the advantage the seed layer etch-back can be an unpatterned etch in chrome etchant.

While both methods were used to successfully pattern a circuit shield for active probes, it turns out that both methods produced an unwanted side effect which had to be addressed. Prior to sputtering the seed layer, it is necessary to carry out a short (10 second) BHF dip in order to clear the native oxide from the contacts in the bond pads or beam lead areas. It is suspected that this quick BHF dip etched back enough LTO in the circuit area to expose small protrusions of underlying circuit metal (discussed more fully in the following subsection) which resulted from liftoff. For this reason, it is desirable to carry out the plating of the circuit area separately from metalization of the bond pads or beam leads. In this way, the BHF dip can be avoided in the circuit area where it is not needed and can potentially lead to harm. In order to accomplish this, bond pads and beam leads are first created using liftoff of sputtered chrome/gold. A BHF dip is used to clear native oxide in the contact areas, while the circuit area is protected by the dark-field liftoff mask. Following liftoff, a chrome/gold/chrome seed layer is sputtered, and electroplating is carried out with a photoresist mold as with the first method above. This process is the most complicated of the three discussed, but appears to be necessary to avoid the pitfalls so far observed with this process.

4.3 Circuit Metalization

It was mentioned above that the blanket BHF dip carried out prior to seed layer sputtering for electroplating exposed spikes of the circuit metal which penetrated the LTO passivation layer. These spikes were observed to short the circuit metal to the shield, which is obviously intolerable. It is believed that the changes to the electroplating process described above will solve this problem. In addition, the circuit metalization process was re-characterized in order to minimize the presence of these spikes, and commercially available photoresists which are supposed to solve this problem are being explored.

Figure 8 illustrates the basic problem, which is that the sputtered metal film adheres to the sloping photoresist sidewall. During liftoff, the metal lines often separate

at the top, rather than the bottom, of the sidewall. Mechanical scrubbing of the wafer during liftoff in an ultrasonic shaker improves the situation, but does not appear to remove all spikes even after several hours of shaking.

It is not known whether the spikes have been present in recent active probe runs but went unobserved or whether the BHF dip associated with the electroplated gold circuit shield (discussed above) exacerbated this problem. Because the etch rate of aluminum in EDP can be less than 0.1µm per hour (depending upon the exact formulation) it is possible that some degree of spiking has been present but went unobserved as the relatively thin and narrow spikes were attacked vertically in EDP. It is possible, then, that the presence of the gold circuit shield is a more strenuous test of circuit encapsulation than is successful etch-out in EDP.

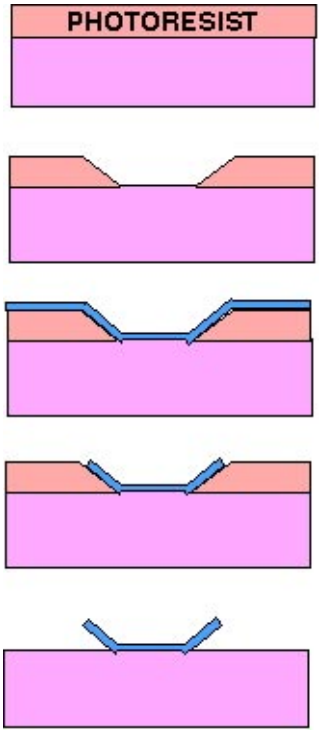

Fig. 8: Standard lift-off process leading to sidewall spikes.

Figure 9 shows a typical metal line with spikes clearly in evidence, especially under magnification. The metalization process used was to spin 1827 photoresist, expose with a dark field mask, and sputter approximately 7000Å of metal. Similar results were obtained regardless of whether the metal was lifted off with an overnight soak in acetone and ultrasonic scrubbing, or soaking for 1-2 hrs in hot 1112A (an organic solvent with surfactant) and ultrasonic scrubbing.

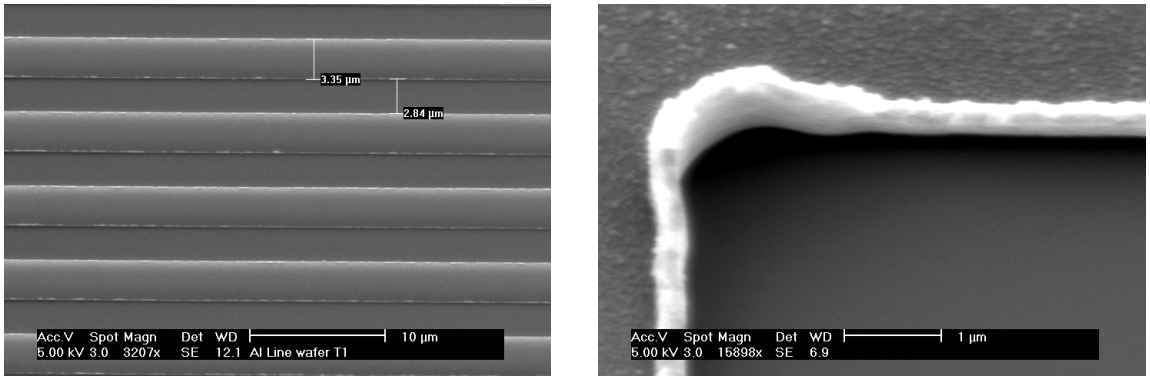

Fig. 9: Circuit metal lines showing evidence of vertical spiking along edges. Spikes tended to be especially serious at inside corners, magnified at right.

The first step in the resolution of this problem was to fully characterize the liftoff process in order to determine a set of parameters that would minimize spiking. Because the spiking is related to metal sidewall adhesion, it was postulated that the severity of spikes could be minimized by controlling the sidewalls of the photoresist. It was thought that resist thickness would have some effect on sidewall adhesion. In addition, the steepness of the sidewall was expected to play a role in the degree of adhesion.

Figure 10 shows the sidewall profile of 1827 photoresist prior to sputtering metal. While the sidewall is relatively steep, the right-hand SEM shows the significant rounding of the sidewall that occurs during a one minute oxygen plasma descum step. The descum step is necessary with this lithography process in order to clean out undeveloped resist in the contact holes prior to metalization. The rounding is most pronounced at the corners, which might explain why the spikes were most prominent there.

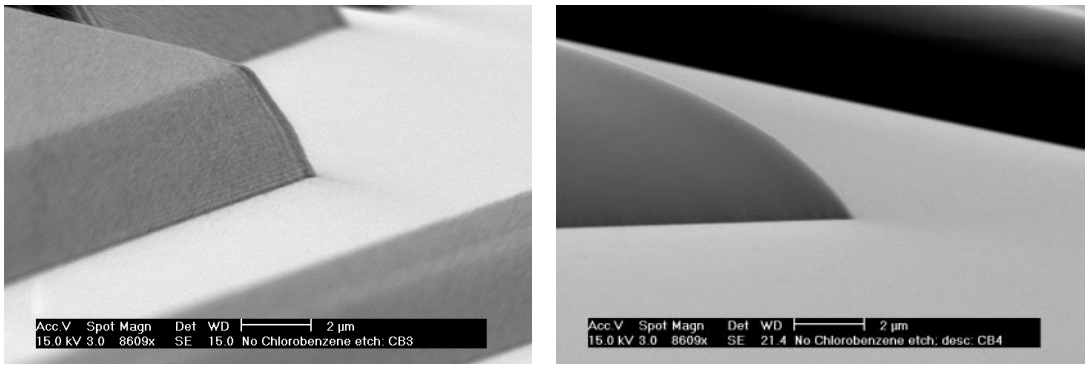

Fig. 10: PR1827 photoresist profile before (left) and after (right) plasma descum.

One potential solution to this problem is to use surface treatments to create an overhang in the resist profile. This is reported to make liftoff more rapid and clean. Using a 20 minute chloro-benzene soak prior to exposing and developing the 1827 resist, we were able to create fairly dramatic photoresist overhangs (Fig. 11). In fact, the liftoff process proceeded very rapidly and was competed in a fraction of the usual time.

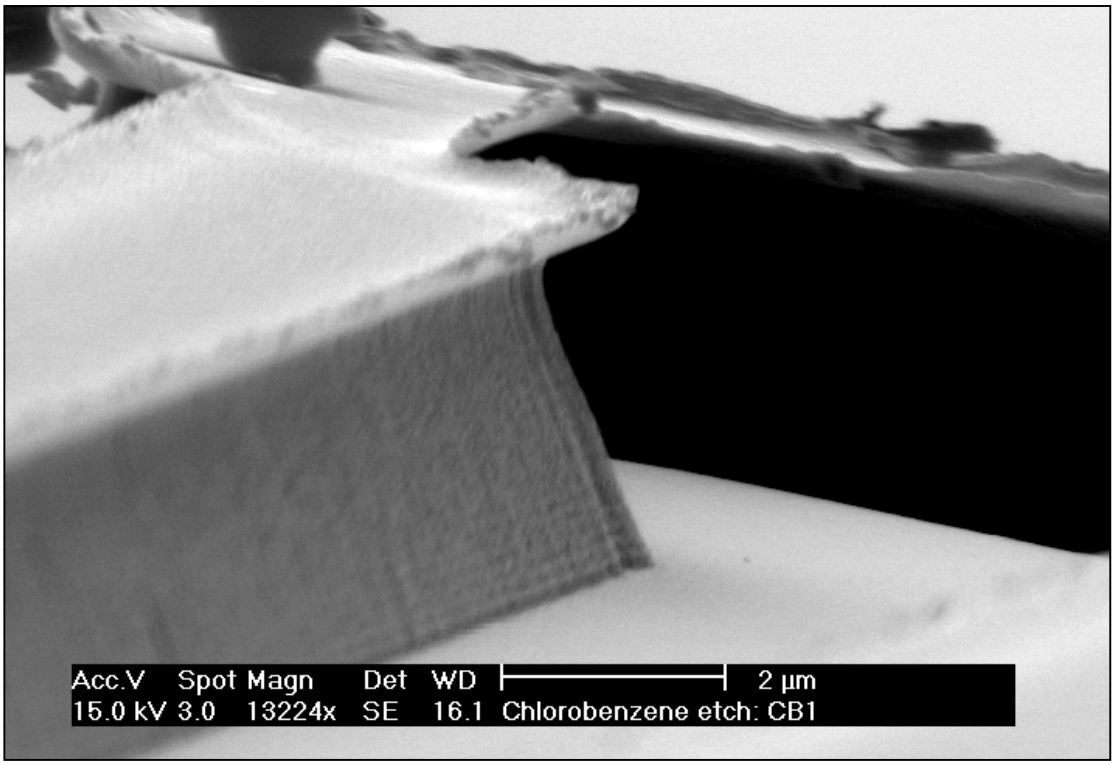

Fig. 11: Photoresist overhang created with chloro-benzene.

However, the use of chlorobenzene did not seem to improve the problem of metal spiking after liftoff. It is likely that the overhang interfered with metal adhesion near the top of the sidewall, but still allowed metal to adhere conformally closer to the bottom. This would allow encourage the metal to break near the top during liftoff, which does nothing to solve the original problem.

These observations suggest that using image reversal with AZ-5214 photoresist might offer several advantages in the metalization process. First, it is known that it is possible to obtain very steep or even inverted sidewall profiles with image reversal. Second, with image reversal, the photoresist in the metal lines is cleared with a flood exposure, which is generally a very long exposure time.

Metal lines using 5214 spun on the wafer at 1500, 3000, and 4000rpm were evaluated. It was determined that the thicker resist produced more favorable results. Next, a matrix of exposure, flood and develop times was set up in order to optimize the sidewall steepness. The resulting sidewall profiles were evaluated using an SEM. Figure 12 shows exposure times of 5, 10 and 15 seconds (left to right) and flood exposures of 30 and 60 seconds (top and bottom respectively.) The effect on the sidewall steepness is apparent, with the best profiles obtained at higher exposures and floods. However, it is important to note that the line thickness (horizontal extent) is also under the control of the initial exposure and thus exposure cannot be optimized completely independently without redesigning the metal mask and biasing the drawn line thicknesses. As a result, it was

found that initial exposures on the order of 8-10 seconds were optimum for greatest line width control and sidewall steepness.

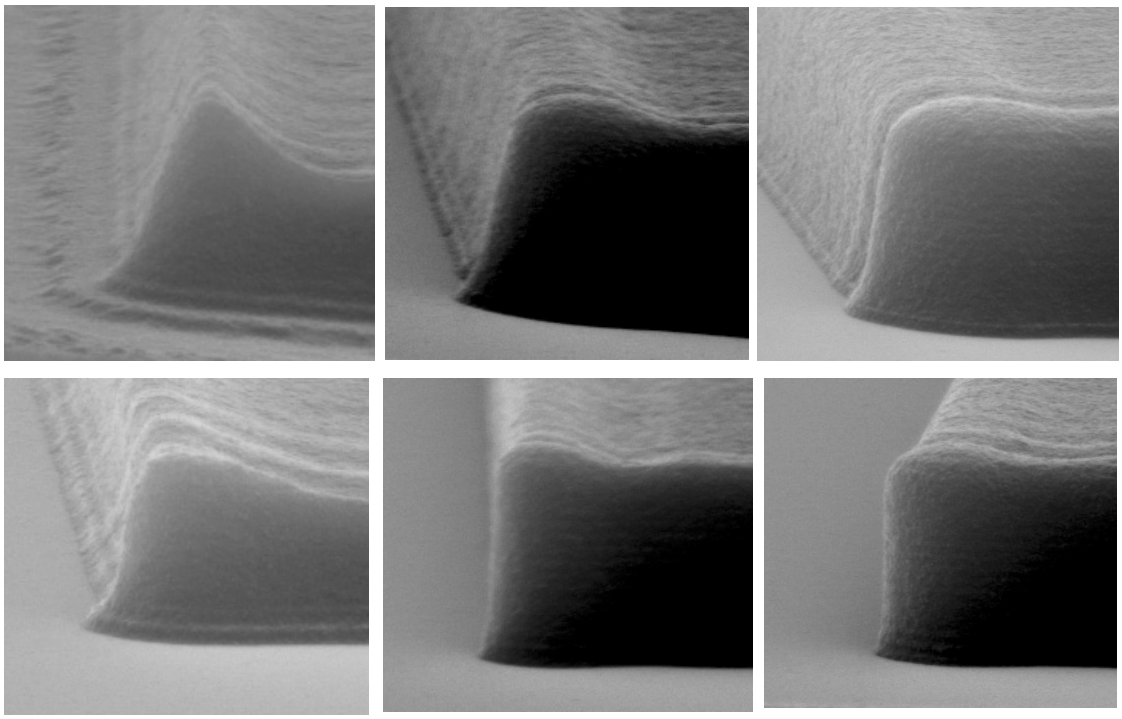

Fig. 12: AZ-5214 sidewall profiles with 5, 10, and 15 second exposures (left to right) and 30 and 60 second flood exposures (top and bottom, respectively.)

The problem with spikes in metal films resulting from liftoff is well-known in commercial IC foundries, and a solution has been developed using a two-layer photoresist called liftoff resist (LOR) which produces an undercut profile as shown in Fig. 13. This provides a discontinuity in the sputtered film and allows the metal to lift off cleanly. Because there are some special processing requirements associated with LOR, it is currently being evaluated for introduction into the laboratory and will be tested and characterized for future use.

4.4 Chronic Active Probe Testing

A family of probes has been designed and fabricated to test and improve the ability of active Michigan probes to record chronically. These probes will allow the measurement of a mean time to failure for different aspects of probe functionality. Test structures have been designed to monitor the etching of circuit metal and polysilicon, to look for theshold shifts under thermal and electrical bias, and to measure leakage currents from metal and polysilicon to saline. In addition, the chronic probes have 8 recording sites that are front-end-selected onto a single buffered output channel to test overall probe

functionality. This probe has been tested exhaustively and is functioning as expected. The on-chip buffer is a unity-gain operational amplifier. This buffer has the advantages of lower output resistance, less DC offset, and gain closer to one than the previously used source follower.

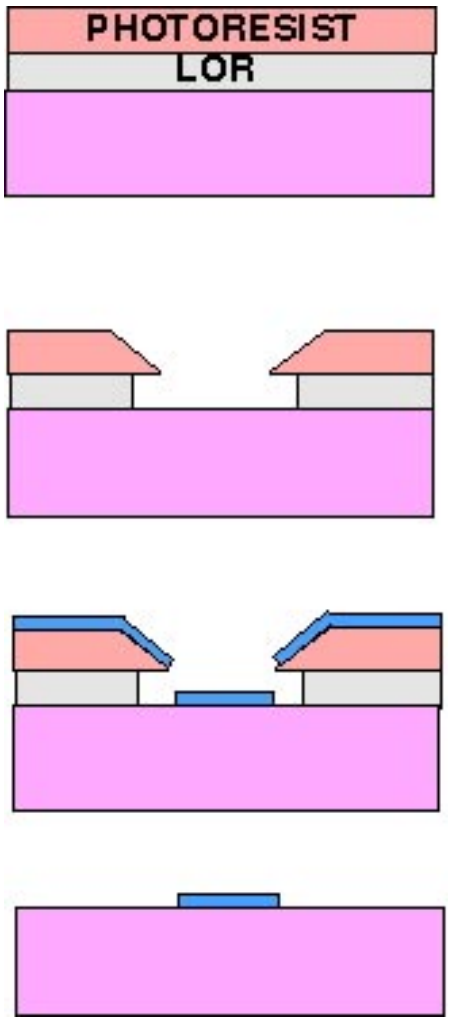

Fig. 13: Metal liftoff using two-layer LOR.

In-vitro testing of these probes at body temperature with a subset of the measurable parameters on a single device has been initiated. Interconnect and test set-up are being completed to allow measurement of all parameters on a larger sample of devices. Accelerated testing of the devices is also planned, along with chronic in-vivo implantation. The initial probe parameters under test are summarized in Table 2, below.

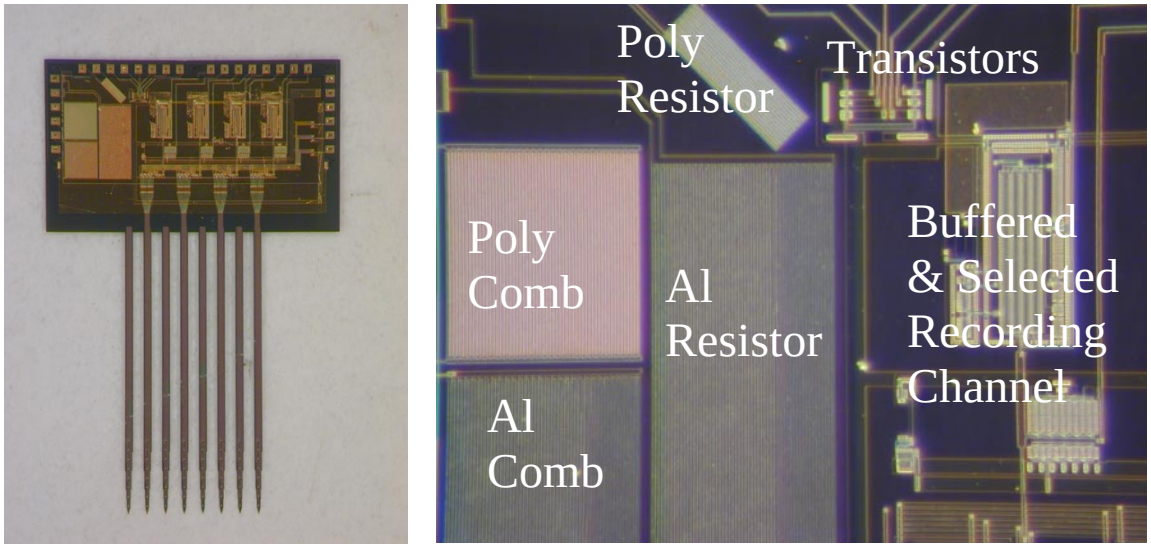

Fig. 14: Fully fabricated probe designed for chronic implantation in guinea pig auditory cortex, left. Detail of test circuitry, at right.

Test Circuit Parameter	Baseline Value (day 0 soak test)
Al resistor value	21-24 kΩ
Poly resistor value	28-28 kΩ
NMOS threshold	0.9V
PMOS threshold	-0.6 – -0.7V
Channel One recording	YES
Channel Two recording	YES
Channel Three recording	YES
Channel Four recording	YES

Table 2: Summary of chronic probe test parameter values on day zero of implantation at 37°C.

5. Development of On-Platform Signal Processing for Chronic Recording Probes

Wafer level testing of the new active neural electrodes (PIA-2) has produced very promising results. The counter used to control the time-division multiplexer has been tested at the wafer level and is fully operational. In addition, other digital circuits such as logic gates and CMOS switches have been tested and are functional. The on-chip amplifiers have also been tested at the wafer level. The gain of the amplifier versus frequency is shown in Fig. 15 below. The in-band gain of the amplifier is 39.5dB with an upper cut-off frequency of 40kHz. The low frequency cut-off is below 10Hz (the low end operating frequency of our gain/phase analyzer) and the amplifier can reject greater

than ±400mV of DC at its input. The response of the preamplifier to a 5mV 1kHz sine wave is pictured in Fig. 16.

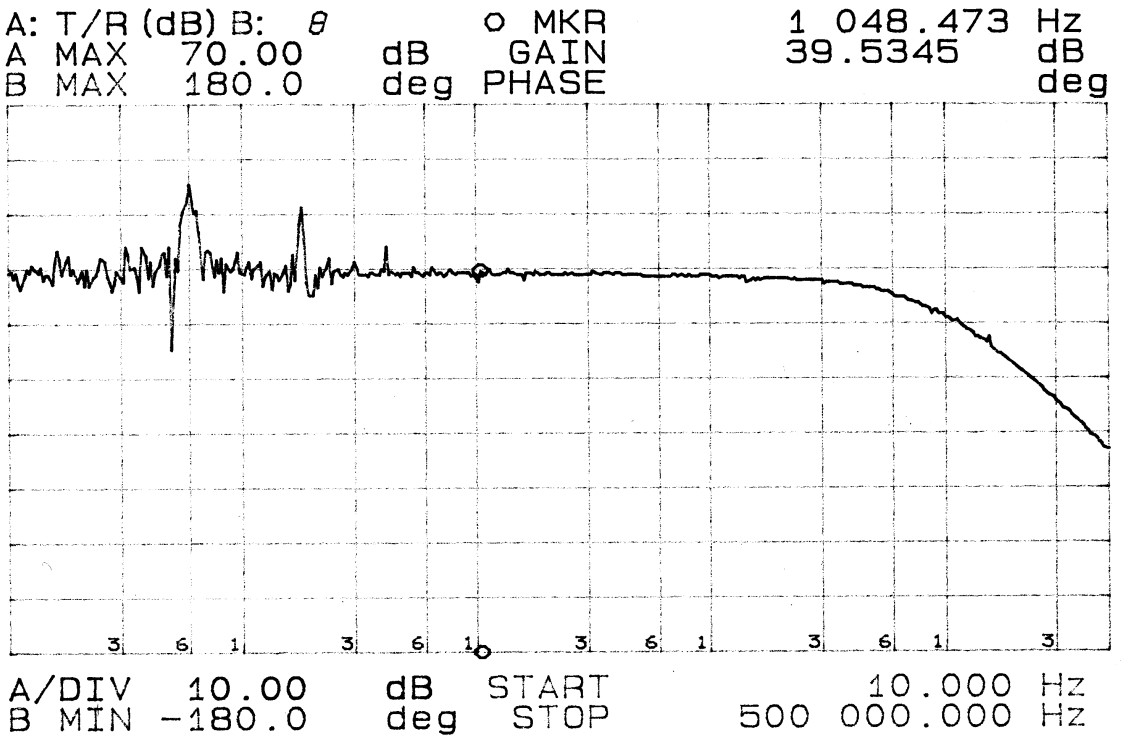

Fig. 15: Preamplifier Gain vs. Frequency

Preliminary system level testing has also been conducted at the wafer level. The PIA-2 64-site, eight channel active neural recording probe operates from a 3V supply and consumes 822µW of power. In order to conduct some initial tests before bonding, the probe was placed in test mode and the response of the system to a 2mV 1kHz sinusoid was measured. This test signal was coupled into the inputs of the preamplifiers. The time-division multiplexer was statically set up during this test to pass the output of the first preamplifier to the active filter, which adds an additional gain of 10dB to all the channels. The results of this test are shown in Fig. 17.

The development of the platform-mounted spike detection unit is being pursued and should be completed prior to the MOSIS AMI 0.5µm process run scheduled to begin February 25th. In order to make the design easier to test, it has been broken into four separate units: a comparator array, an address counter, an output register, and a spike detector (note the entire design will be simulated together, breaking up the design into segments allows for internal signals to be easily routed to pads for testing). The behavioral verilog source codes for the address counter, spike detector and output register have been completed and simulated individually and together to ensure functionality. The address counter and spike detector blocks have been synthesized to produce

transistor level schematics for both designs. From these schematics, structural level verilog files have been generated and simulated to verify that no errors occurred during synthesis. Using silicon ensemble and the structural verilog files, layouts of the address counter (Fig. 18) and the spike detector (Fig. 19) have been produced and checked for design rule and lvs errors. The address counter occupies 650µm X 650µm of die area while the much larger spike detector block consumes 3.5mmX3.5mm of die space.

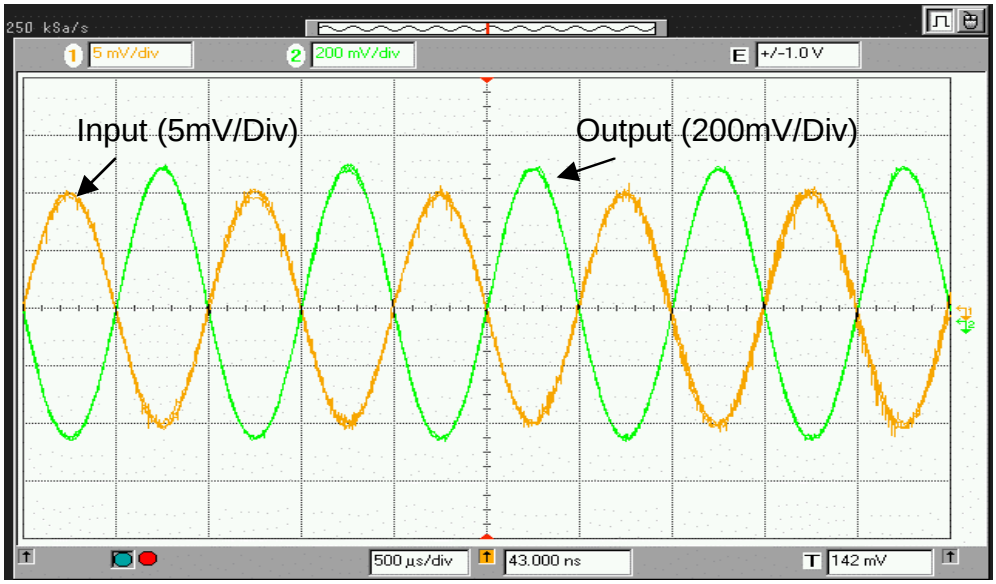

Fig. 16: Preamplifier response to 1kHz sinusoid

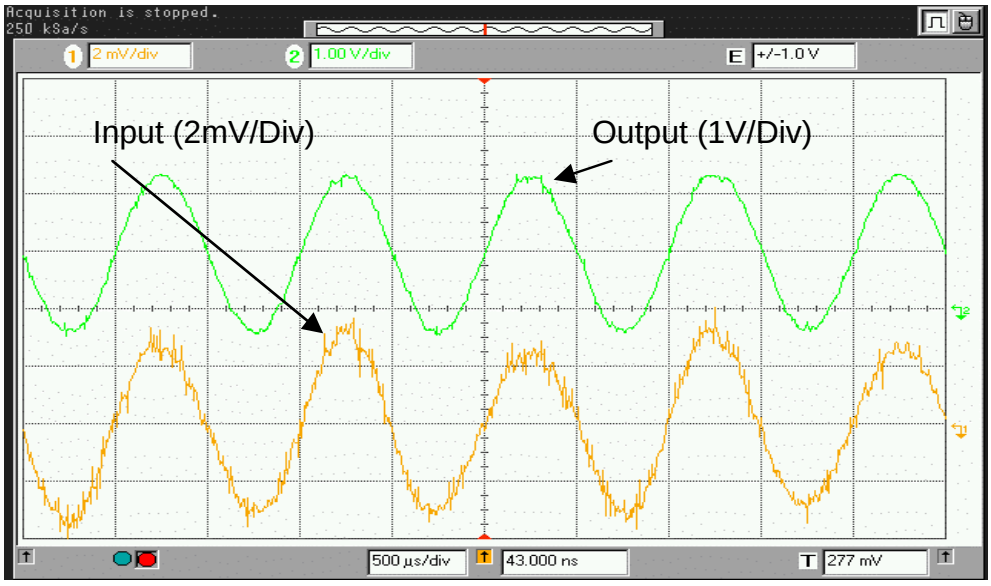

Fig. 17: System response to a 1kHz sinusoid

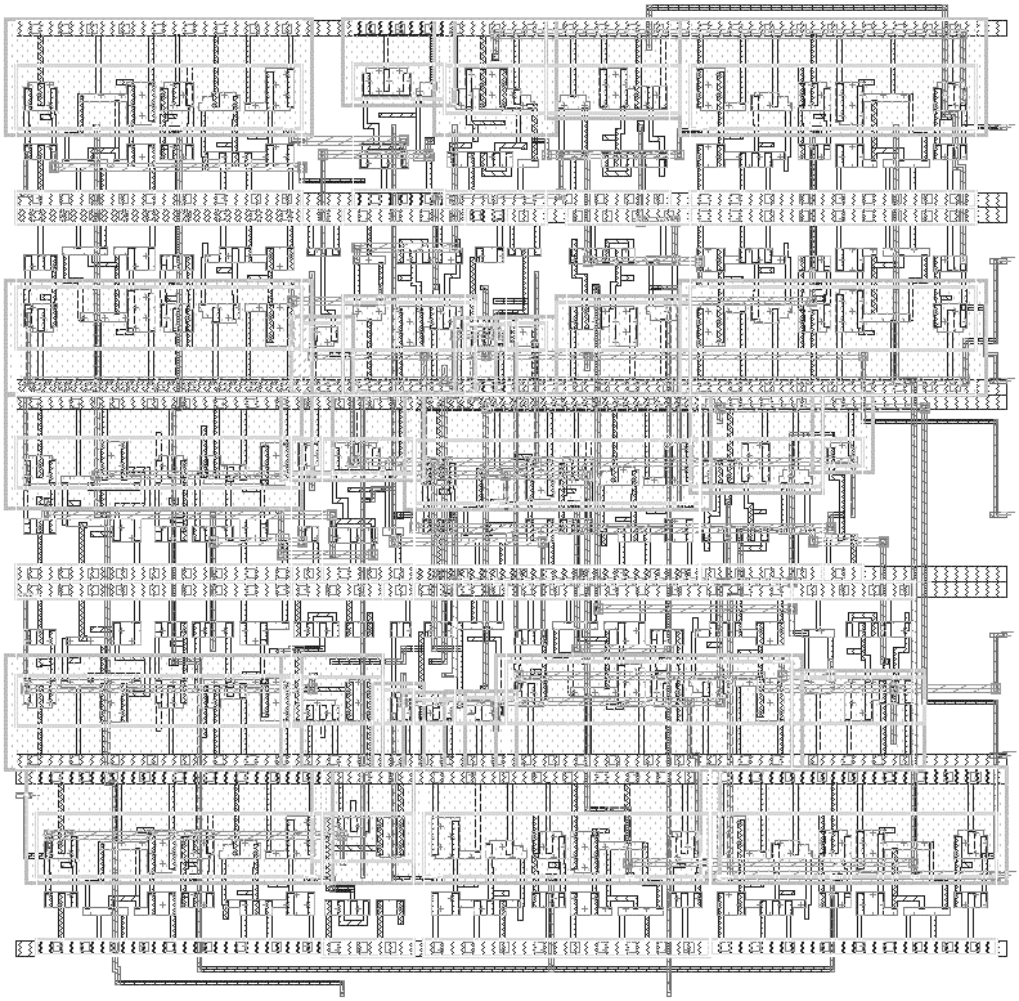

Fig. 18: Layout of the address counter

6. Design of a Wireless Telemetry Platform for Multichannel Microprobes

We have now completed the design, fabrication, and testing of the front-end circuitry and A/D module for the platform-mounted telemetry interface being designed for the active recording probes. The next step has been to design the data link, including the implanted transmitter and external receiver. The following tasks were carried out during this past quarter:

Analysis of the Sigma-Delta Modulator (SDM)
Design of the data link.

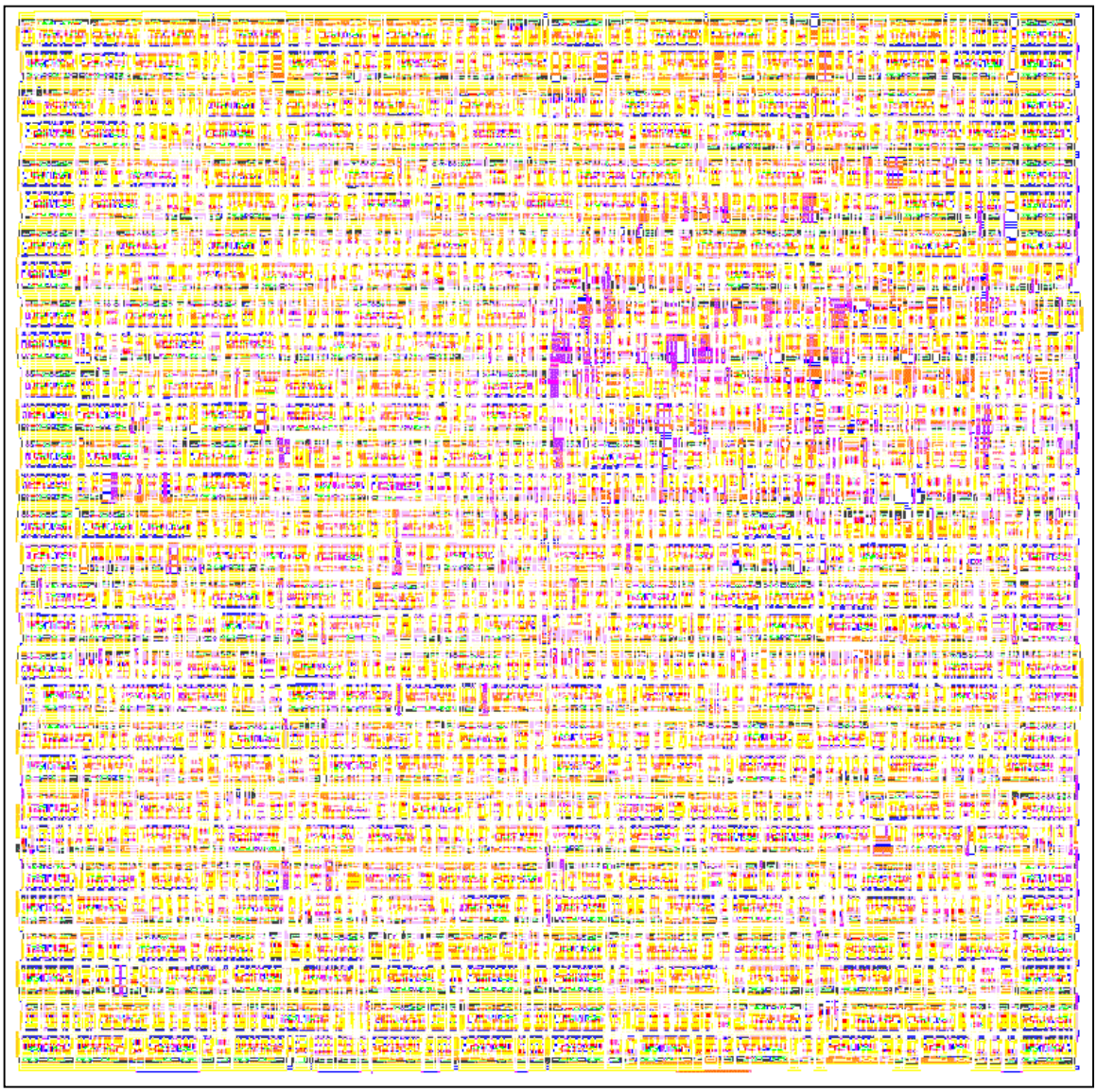

Fig. 19: Spike detector

6.1 Analysis of the Sigma-Delta Modulator

The resolution of the SDM was measured using the following method. A pure sinusoid of 1kHz was fed to the SDM run at a clock of 200kHz, and the output of the SDM was recorded for more than 100ms. Midas3 was used to reconstruct the original signals and calculate the spectra of the reconstructed sinusoid, shown in Fig 20.

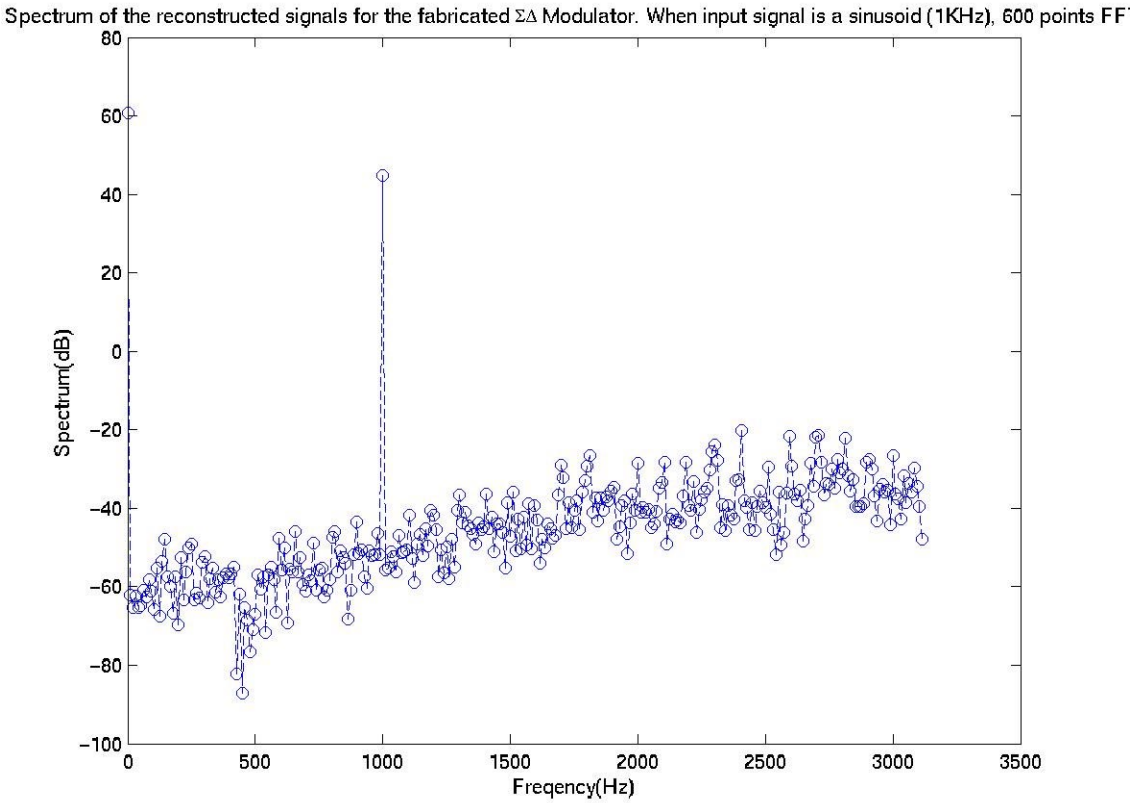

Fig. 20: The spectra of reconstructed 1kHz sinusoid based on 600 points FFT, M=64

Different down-sampling ratios were used to understand their effect on the resolution, and Midas3 was used to calculate the SNDR for different down-sampling ratios.

For an N-bit ideal ADC, the signal-to-quantization-noise ratio, or dynamic range, can be shown as

$$SNR(dB) = 6.02N + 1.76dB \qquad (1)$$

The derivation is as following: If the input range of ADC is from 0 to V_{max}, the least-significant-bit (LSB) voltage is $V_{lsb} = V_{max}/2^N$ for N-bit ADC. Because the width of each code step is identical and has an equal probability for an ideal ADC, the magnitude of quantization error V_q should fall into the range of $[0, V_{lsb}/2]$ with equal possibility, i.e., V_q has a uniform PDF (probability density function) in $[0, V_{lsb}/2]$. Then the quantization noise P_q, average of $|V_q|^2$, is $V_{lsb}^2/12$ based on probability theory. If sinusoidal signal is fed to the ADC, the maximum peak-to-peak amplitude should be V_{max} in order that ADC can handle without overload. Then, the power of the input sinusoid is $P_{in} = V_{max}^2/8$. Consequently, the SNR of N-bit ADC is

$$SNR = 10\log\frac{P_{in}}{P_q} = 10\log\frac{12\times 2^{2N}}{8} = 6.02N + 1.76dB \quad (2)$$

For the fabricated SDM, calculated SNDR=51.46dB for M=32, which means 8-bit accuracy. For M=64, the calculated SNDR=64.28dB, corresponding to 10-bit accuracy. Obviously, larger over-sampling ratios lead to higher resolution in sigma-delta A/D conversion as well as lower conversion speed.

The power source of the sigma-delta modulator is from the on-chip regulator and the power consumption of the sigma-delta modulator is about 230μW.

As discussed in previous reports, an SDM can be used to digitize the neural signals in order to achieve 10-bit resolution even though RF powering may couple noise to the substrate of the implanted chip. This A/D conversion is fairly suitable in one channel neural recording. If this type of A/D converter is adopted in multi-channel recording, a multiplexer may not be used on the probe to sample different channels (time division method), since oversampling is necessary for every channel in Sigma-Delta A/D Conversion. However, multiple SDMs can be used for multi-channel A/D conversion, with every SDM corresponding to one neural channel. More interconnections may be needed from the non-multiplexed channels on the probe to the platform-mounted A/D circuitry.

6.2 Design of Data Link

RF Transmitter Design

The most important issue of [1]an implanted biotelemetry system is power dissipation. To minimize the power of a transmitter, we have to select the lowest practical RF carrier frequency, since RF circuits dissipate power that is proportional to their operating frequency.

The FCC has authorized unlicensed use of the 38-41MHz, 88-108MHz, and 174-216MHz Very High Frequency (VHF) bands for Industrial, Scientific and Medical (ISM) telemetry purposes [1]. Other bands in the microwave region (900MHz and above) are not considered because of high tissue absorption at those frequencies. On the other hand, a higher carrier frequency is desired for wider bandwidth in data transmission. As the result of these trade-offs, ~200MHz is chosen as the carrier frequency. Another major concern is also the effect on tissue of a strong RF field. To avoid tissue damage due to RF heating, the maximum RF power density should not exceed 10mW/cm^2 [2]. These

[1] Federal Communication Commission, *FCC rules and regulations , part 15*

[2] P.A. Neukomm, "Health hazards for telemetry RF exposure? A review on the interactions between electromagnetic fields and biosystems**"**, *Biotelemetry III, Proc. Int'l Symp. on Biotelemetry, pp. 41-44, Academic Press, 1976*

constraints are not difficult to meet given that the required transmitted power is in the order of microwatts for experiments.

As reported by B. Ziaie, a 600μW implantable transmitter was designed for biotelemetry at bit rate of 1Mbps, where a Colpitts oscillator was built on that transmitter. We can continue to use the circuit architecture, shown in Fig. 21. It is expected that a 1mW implantable transmitter with the same principle can achieve a bit rate of 1.6Mb/s for 8-channel neural recording.

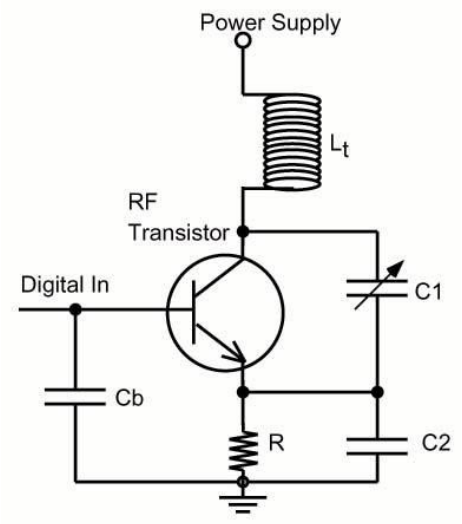

Fig. 21: On-chip hybrid transmitter

C_1 in Fig. 21 is the tuning capacitor, and the frequency is determined by L_t, C_1 and C_2 as in Equation (3),

$$f = \frac{1}{2\pi\sqrt{L_t \dfrac{C_1 C_2}{C_1 + C_2}}} \qquad (3)$$

so the transmitter can be tuned to various frequency by laser trimming C_1.

The input of the RF transmitter comes from a FIFO data buffer, where A/D conversion results are stored as well as a header and CRC block added by transmission control logic.

Overview of the external receiver

Because the transmission scheme of the on-chip transmitter is OOK, it can be regarded as a special amplitude modulation. Thus, the external receiver can be easily implemented as an envelope detector. The block diagram is shown in Fig. 22.

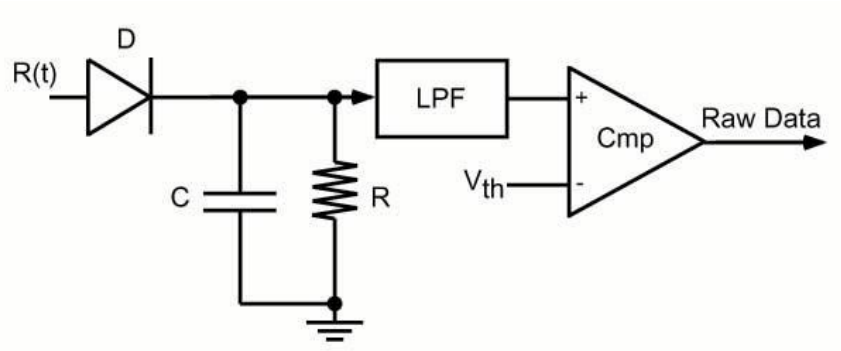

Fig. 22: The block diagram of an external envelop detector

Diode D, R and C in Fig. 22 form a simple envelope detector, and we set the R and C according to (4)

$$\frac{1}{f_c} << RC << \frac{1}{f_m} \qquad (4)$$

where f_c is carrier frequency, and f_m is data transmission rate. The output raw data is then fed to computers or other logic circuitry for CRC check and decoding.

If data transmission scheme is one of other more complex schemes such as Binary Phase Shift Keying (BPSK) or Quadrature Phase Shift Keying (QPSK)[2], it can result in higher data rates than OOK under the same conditions of SNR and P_e(error probability). The PLL can be designed to retrieve coherent signals used in demodulation where discrete IC components of the PLL are commercially available.

7. Conclusions

During the past quarter, we have continued to improve our packaging techniques for chronic recording probes and have begun, working with the Center for Neural Communication Technology, to explore the tissue reaction to chronically implanted probes using a new round of histological studies. We have also begun to design narrow-shank recording probes using both single-crystal silicon and polysilicon shank structures. The anticipated probes will have multiple shanks, each about 3µm wide, with recording sites that overhang the shank to allow full-field recording in-vivo. The chronic behavior of the new sites will be studied in the potential field of single cells.

Fabrication has been completed through final release on a samples of the most recent probe designs. The wafer yield was excellent, with very few broken shanks and almost no evidence of circuit undercutting. Probes appear to be functioning as designed, with several probes bonded and in-vitro and in-vivo testing underway. Release on standard probe designs is now straightforward; however, care must be taken in probe placement on the wafer and in the release etch when shank spacings less than 150µm are used. A dry silicon etch is one approach that has been found effective in fabricating the smaller structures. Gold shields have been fabricated over the circuit areas of some of the new active probes. The circuitry is functional and these probes are being applied to long-term testing in-vivo and (at higher temperatures) accelerated testing in-vitro.

In releasing some of the active probes, problems with metal spikes remaining at the patterned metal edges after lift-off have been seen. Extensive photoresist studies of the line edges during lift-off have been carried out and have suppressed these problems adequately to achieve acceptable probe yields. A new photoresist specifically designed for use in lift-off processes has also been obtained and will be explored as a more complete solution to the problem.

Wafer level testing of the newly-designed active probes (PIA-2) has produced very promising results. The counter used to control the time-division multiplexer is fully operational along with associated logic gates and CMOS switches. The capacitively-coupled PIA-2 on-chip amplifiers have also been tested at the wafer level. The in-band gain is 39.5dB with an upper cut-off frequency of 40kHz. The low frequency cut-off is below 10Hz; the amplifier can reject greater than ±400mV DC at its input. Design of a platform-mounted integrated circuit that will perform neural spike detection based on a user-input threshold is also nearing completion. It is being designed in an AMI 0.5µm CMOS process and will be fabricated as part of a MOSIS run starting late next month.

Finally, the sigma-delta modulator to be used in the first recording probe telemetry interface has been analyzed. The circuit dissipates 230µW and produces 8b resolution for x32 oversampling. We are developing a Colpitts oscillator design for use as the transmitter. It is expected that the 1mW transmitter will achieve a bit rate of 1.6Mb/s for 8-channel neural recording.